

U.S. PATENT DOCUMENTS						
Examiner Initials ¹	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
[Handwritten marks]		6,015,724		Yamazaki	01/18/2000	
		4,033,833		Bestel et al.	07/05/1977	
		5,726,461		Shimada et al.	03/10/1998	
		6,359,320		Yamazaki et al.	03/19/2002	
		5,851,918		Song et al.	12/22/1998	
		5,929,948		Ohuri et al.	07/27/1999	
		6,509,616		Yamazaki	01/21/2003	
		2001/0010370		Kimura et al.	08/02/2001	
		6,413,845		Izumi et al.	07/02/2002	
		6,515,365		Higashi et al.	02/05/2003	
		6,573,602		Seo et al.	06/03/2003	
		6,509,649		Sugai	01/21/2003	
	6,479,900		Shinogi	12/12/2000	11/2002	

[illegible]

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
HD		Stanley Wolf "4.5.6.3 Contact-Hole and Via Filling with Selective Electroless Metal Deposition," Silicon Processing for the VLSI Era, Vol. 2, Process Integration, pp. 256-257	
HD		M. Hatano et al., "A Novel Self-Aligned Gate-Overlapped LDD Poly-Si TFT with High Reliability and Performance," IEDM 97, pp. 523-526	
HD		U.S. Patent Application Serial No. 10/245,701 entitled Semiconductor Device and Method of Manufacturing the Same filed 09/18/2002	

Examiner Signature	<i>Hendler G. Okey</i>	Date Considered	<i>10/3/03</i>
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.